

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	09989762
Filing Date	2001-11-19
First Named Inventor	Kenneth Y. Ogami
Art Unit	2123
Examiner Name	Osborne, Luke R.
Attorney Docket Number	CD01175M

U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7042301	B1	2006-05-09	Sutardja, Sehat	Entire Document
	2	5594388	B1	1997-01-14	O'Shaughnessy et al.	Entire Document
	3	5963105	B1	1999-10-05	Nguyen	Entire Document
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10	7250825	B1	2007-07-31	Wilson et al.	Entire Document
11	7200507	B1	2007-04-03	Chen et al.	Entire Document
12	7421251	B1	2008-09-02	Westwick et al.	Entire Document
13	7542533	B1	2009-06-02	Jasa et al.	Entire Document
14	7154294	B1	2006-12-26	Liu et al.	Entire Document
15	6809566	B1	2004-10-26	Xin-LeBlanc, Jane	Entire Document
16	6154064	B1	2000-11-28	Proebsting, Robert J.	Entire Document
17	6037807	B1	2000-03-14	Wu et al.	Entire Document
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20	4885484	B1	1989-12-05	Gray	Entire Document
21	5432476	B1	1995-07-11	Tran	Entire Document
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27	6819142	B1	2004-11-16	Viehmann et al.	Entire Document
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31	6924668	B1	2005-08-02	Muller et al.	Entire Document
32	7088166	B1	2006-08-08	Reinschmidt et al.	Entire Document
33	7119602	B1	2006-10-10	Davis	Entire Document
34	7265633	B1	2007-09-04	Stiff, Jonathon	Entire Document
35	11322044	B1	2005-12-28	Stiff, Jonathon	Entire Document
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38	5748048	B1	1998-05-05	Moyal	Entire Document
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43	6026134	B1	2000-02-15	Duffy et al.	Entire Document
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45	6211741	B1	2001-04-03	Dalmia	Entire Document
46	6275117	B1	2001-08-14	Abugharbieh et al.	Entire Document
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	1	Application Number 11/850,260 (CD2007006): "Circuit and Method for Improving the Accuracy of a Crystal-Less Oscillator Having Dual-Frequency Modes;" Wright et al.; 33 pages	<input type="checkbox"/>
	2	USPTO Non-Final Rejection for Application Number 11/850,260 (CD2007006) dated 03/06/2009; 7 pages	<input type="checkbox"/>
	3	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 03/09/2009; 11 pages	<input type="checkbox"/>
	4	USPTO Advisory Action for Application Number 11/644,100 (CD05204) dated 02/09/2009; 3 pages	<input type="checkbox"/>
	5	USPTO Final Rejection for Application Number 11/644,100 (CD05204) dated 11/18/2008; 12 pages	<input type="checkbox"/>
	6	USPTO Non-Final Rejection for Application Number 11/644,100 (CD05204) dated 04/14/2008; 10 pages	<input type="checkbox"/>
	7	USPTO Notice of Allowance for Application Number 11/415,588 (CD05028) dated 03/11/2008; 6 pages	<input type="checkbox"/>

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8	USPTO Advisory Action for Application Number 11/415,588 (CD05028) dated 01/14/2008; 3 pages	<input type="checkbox"/>
9	USPTO Final Rejection for Application Number 11/415,588 (CD05028) dated 10/19/2007; 8 pages	<input type="checkbox"/>
10	USPTO Non-Final Rejection for Application Number 11/415,588 (CD05028) dated 06/13/2007; 8 pages	<input type="checkbox"/>
11	USPTO Notice of Allowance for Application Number 12/218,404 (CD05028C1) dated 03/19/2009; 7 pages	<input type="checkbox"/>
12	USPTO Non-Final Rejection for Application Number 12/218,404 (CD05028C1) dated 09/30/2008; 8 pages	<input type="checkbox"/>
13	Application Number 11/644,100 (CD05204): "Differential-to-single ended signal converter circuit and method," Stiff, 33 pages	<input type="checkbox"/>
14	Application Number 11/415,588 (CD05028): "Voltage Controlled Oscillator Delay Cell and Method," Sivadasan; 24 pages	<input type="checkbox"/>
15	Application Number 12/218,404 (CD05028C1): "Voltage Controlled Oscillator Delay Cell and Method," Sivadasan; 23 pages	<input type="checkbox"/>
16	USPTO Notice of Allowance for Application Number 11/132,894 (CD04064) dated 04/26/2007; 4 pages	<input type="checkbox"/>
17	USPTO Non-Final Rejection for Application Number 11/132,894 (CD04064) dated 12/19/2006; 12 pages	<input type="checkbox"/>
18	Application Number 11/132,894 (CD04064): "Open Loop Bandwidth Test Architecture and Method for Phase Locked Loop (PLL)," Stiff, 38 pages	<input type="checkbox"/>

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19	USPTO Non-Final Rejection for Application Number 11/322,044 (CD05198) dated 05/04/2009; 18 pages	<input type="checkbox"/>
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21	USPTO Non-Final Rejection for Application Number 11/322,044 (CD05198) dated 04/11/2008; 11 pages	<input type="checkbox"/>
22	USPTO Advisory Action for Application Number 11/322,044 (CD05198) dated 11/30/2007; 2 pages	<input type="checkbox"/>
23	USPTO Final Rejection for Application Number 11/322,044 (CD05198) dated 09/21/2007; 14 pages	<input type="checkbox"/>
24	USPTO Non-Final Rejection for Application Number 11/322,044 (CD05198) dated 04/24/2007; 13 pages	<input type="checkbox"/>
25	Application Number 11/322,044 (CD05198): "Split charge pump PLL architecture," Stiff; 19 pages	<input type="checkbox"/>
26	USPTO Notice of Allowance for Application Number 10/305,589 (CD02181) dated 02/04/2005; 5 pages	<input type="checkbox"/>
27	USPTO Final Rejection for Application Number 10/305,589 (CD02181) dated 10/21/2004; 7 pages	<input type="checkbox"/>
28	USPTO Non-Final Rejection for Application Number 10/305,589 (CD02181) dated 10/07/2003; 6 pages	<input type="checkbox"/>
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30	Application Number 09/849,164 (CD01035): "Reduced Static Phase Error CMOS PLL Charge Pump," Stiff, 30 pages	<input type="checkbox"/>
31	Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996; 10 pages	<input type="checkbox"/>
32	Larsson, "A 2-1600-MHz CMOS Clock Recovery PLL with Low-V _{dd} Capability," IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999; 10 pages	<input type="checkbox"/>
33	USPTO Notice of Allowance for Application Number 10/327,217 (CD02174) dated 08/12/2004; 6 pages	<input type="checkbox"/>
34	USPTO Non-Final Rejection for Application Number 10/327,217 (CD02174) dated 04/30/2004; 5 pages	<input type="checkbox"/>
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36	Application Number 10/327,217 (CD02174): "Single Ended Clock Signal Generator Having a Differential Output," Richmond et al.; 27 pages	<input type="checkbox"/>
37	USPTO Notice of Allowance for Application Number 10/871,582 (CD03036) dated 03/30/2006; 6 pages	<input type="checkbox"/>
38	USPTO Final Rejection for Application Number 10/871,582 (CD03036) dated 02/01/2006; 5 pages	<input type="checkbox"/>
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41	USPTO Notice of Allowance for Application Number 09/404,891 (CD99054) dated 03/04/2005; 6 pages	<input type="checkbox"/>
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43	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 06/25/2004; 6 pages	<input type="checkbox"/>
44	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 01/05/2004; 5 pages	<input type="checkbox"/>
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47	USPTO Non-Final Rejection for Application Number 09/404,891 (CD99054) dated 10/11/2002; 5 pages	<input type="checkbox"/>
48	Application Number 09/404,891 (CD99054): "Method, Architecture and Circuitry for Controlling Pulse Width in a Phase and/or Frequency Detector," Scott et al.; 17 pages	<input type="checkbox"/>
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	1	6636096	B1	2003-10-21	Schaffer et al.	Entire Document
	2	6560306	B1	2003-05-06	Duffy et al.	Entire Document
	3	6680632	B1	2004-01-20	Meyers et al.	Entire Document
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15	6917661	B1	2005-07-12	Scott et al.	Entire Document
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23	6614374	B1	2003-09-02	Gustavsson et al.	Entire Document
24	6670852	B1	2003-12-30	Hauck	Entire Document
25	6625765	B1	2003-09-23	Krishnan	Entire Document
26	6433645	B1	2002-08-13	Mann et al.	Entire Document
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28	5684434	B1	1997-11-04	Mann et al.	Entire Document
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33	6980060	B1	2005-12-27	Boerstler et al.	Entire Document
34	6380811	B1	2002-04-30	Zarubinsky et al.	Entire Document
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36	4980652	B1	1990-12-25	Tarusawa et al.	Entire Document
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49	6043719	B1	2000-03-28	Lin et al.	Entire Document
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	1	Application Number 10/226,911 (CD02112): "Calibration of Integrated Circuit Time Constants," Gehring et al., 32 pages	<input type="checkbox"/>
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	4	USPTO Final Rejection for Application Number 09/943,149 (CD01085) dated 05/07/2003; 10 pages	<input type="checkbox"/>
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6	Application Number 09/943,149 (CD01085): "Method for Phase Locking in a Phase Lock Loop," Moyal et al.; 21 pages	<input type="checkbox"/>
7	Durham et al., "Integrated Continuous-Time Balanced Filters for 16-bit DSP Interfaces," IEEE, 1993; 6 pages	<input type="checkbox"/>
8	Durham et al., "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," IEEE, 1992; 7 pages	<input type="checkbox"/>
9	Durham et al., "High-Linearity Continuous-Time Filter in 5-V VLSI CMOS," IEEE, 1992; 8 pages	<input type="checkbox"/>
10	Application Number 09/047,595 (CD97115): "Roving Range Control to Limit Receive PLL Frequency of Operation," Scott; 35 pages	<input type="checkbox"/>
11	Application Number 09/216,460 (CD98099): "Circuit and Method for Controlling an Output of a Ring Oscillator," Abugharbieh et al.; 21 pages	<input type="checkbox"/>
12	Application Number 09/471,914 (CD99064): "Reference-Free Clock Generator and Data Recovery PLL," Dalmia et al.; 32 pages	<input type="checkbox"/>
13	Application Number 09/471,576 (CD99062): "Reference-Free Clock Generation and Data Recovery PLL," Dalmia; 30 pages	<input type="checkbox"/>
14	Application Number 10/083,442 (CD01264): "Method/Architecture for a Low Gain PLL with Wide Frequency Range," Meyers et al.; 28 pages	<input type="checkbox"/>
15	Application Number 09/470,665 (CD99065): "Digital Phase/Frequency Detector, and Clock Generator and Data Recovery PLL Containing the Same," Dalmia; 26 pages	<input type="checkbox"/>
16	Application Number 09/893,161 (CD00094): "Architecture of a PLL with Dynamic Frequency Control on a PLD," Moore; 32 pages	<input type="checkbox"/>

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17	Application Number 09/608,753 (CD00018): "PLL Lockout Watchdog," Wilson et al.; 24 pages	<input type="checkbox"/>
18	Application Number 09/398,956 (CD99049): "Frequency Acquisition Rate Control in Phase Lock Loop Circuits," Moyal et al.; 35 pages	<input type="checkbox"/>
19	Application Number 09/747,262 (CD00085): "Linearized Digital Phase-Locked Loop," Williams et al.; 9 pages	<input type="checkbox"/>
20	Application Number 09/981,448 (CD01102): "Oscillator Tuning Method," Hauck; 28 pages	<input type="checkbox"/>
21	Application Number 09/538,989 (CD98104): "Memory Based Phase Locked Loop," Krishnan; 27 pages	<input type="checkbox"/>
22	Application Number 09/048,905 (CD95045): "Programmable Clock Generator," Mann et al.; 42 pages	<input type="checkbox"/>
23	Application Number 08/865,342 (CD95045C): "Programmable Clock Generator," Mann et al.; 41 pages	<input type="checkbox"/>
24	USPTO Notice of Allowance for Application Number 10/293,392 (CD02135) dated 03/10/2004; 6 pages	<input type="checkbox"/>
25	USPTO Non-Final Rejection for Application Number 10/293,392 (CD02135) dated 10/16/2003; 6 pages	<input type="checkbox"/>
26	Application Number 10/293,392 (CD02135): "Low Voltage Receiver Circuit and Method for Shifting the Differential Input Signals of the Receiver Depending on a Common Mode Voltage of the Input Signals," Maher et al.; 20 pages	<input type="checkbox"/>
27	USPTO Notice of Allowance for Application Number 10/288,003 (CD02108) dated 01/14/2005; 6 pages	<input type="checkbox"/>

**INFORMATION DISCLOSURE
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Examiner Name	Osborne, Luke R.
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28	USPTO Final Rejection for Application Number 10/288,003 (CD02108) dated 10/06/2004; 6 pages	<input type="checkbox"/>
29	USPTO Non-Final Rejection for Application Number 10/288,003 (CD02108) dated 04/07/2004; 9 pages	<input type="checkbox"/>
30	Application Number 10/288,003 (CD02108): "Low Voltage Differential Signal Driver Circuit and Method," Roper et al.; 30 pages	<input type="checkbox"/>
31	USPTO Notice of Allowance for Application Number 09/989,777 (CD01208M) dated 06/09/2009; 7 pages	<input type="checkbox"/>

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